UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,140	08/07/2001	Ouyang He	22682-06189	3059

758 7590 11/04/2004

FENWICK & WEST LLP
SILICON VALLEY CENTER
801 CALIFORNIA STREET
MOUNTAIN VIEW, CA 94041

EXAMINER	
AN, SHAWN S	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,140	HE ET AL.	
	Examiner	Art Unit	
	Shawn S An	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-32 and 38-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40* is/are allowed.

6)☒ Claim(s) *17-32,38 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/12/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Restriction/Election

1. Applicants' election without traverse the claims of species II corresponding to figure 3 as filed on 8/12/2004 have been acknowledged. Furthermore, Applicants submit that claims 17-32 and 38-40 read on the elected species. Moreover, Applicants cancel claims 1-16 and 33-37.

The requirement is deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 17-24, 27-32, and 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bae et al (6,421,695 B1).

Regarding claims 17, 27, 30, and 38, Bae et al discloses an IDCT circuit for enabling inverse discrete cosine transform of a data block, comprising:

a plurality of cores (Fig. 9, elements 200, 500) each having input data (710, 300) and output data (300, 600), wherein the input data for each core includes external data (Fig. 9, elements u, k).

Bae et al further discloses means for selecting one of input data of the data block received and a sum of the input data and feedback data (230) for providing first output data (Fig. 3, 200);

coupled to the means for selecting, means for determining first partial products (520) based on the input data (k), and the first output data (300) (Fig. 3, 500);

coupled to the means for selecting and the means for determining first partial products, means for determining an intermediate result based on a sum (530) of the first partial products (Fig. 3, 500); and

coupled to the means for selecting, the means for determining first partial products, and means for determining an intermediate result, means for providing the intermediate result as an operand added to second partial product to obtain a final result (530) (Fig. 3, 500).

Bae et al does not specifically disclose means for determining first partial products based on the input data, the first output data, and the feedback data.

However, since Bae et al discloses means for determining first partial products based on the input data and the first output data, and receiving the feedback data from the IDCT core, it would have been obvious to a person of ordinary skill in the relevant art to modify such that first partial products are determined based on the input data, the first output data, and the feedback data as an alternative mathematical manipulation as desired by the designer.

Bae et al also does not specifically disclose the input data for each core also including the output data feedback from selected ones of the cores.

However, Bae et al further discloses the input data for each core also including the output data feedback (to 230, 530) from their respective core.

Furthermore, a DCT circuit enabling forward discrete cosine transform of a data block is considered a reverse processing of the IDCT circuit.

Therefore, it would have been obvious to a person of ordinary skill in the relevant art employing a DCT/IDCT circuit for enabling inverse discrete cosine transform of a data block as taught by Bae et al to modify each input data such that the input data for each core includes output data feedback from selected ones of the cores as an alternative method, just as long as the modified output data is substantially the same as the output data of the original Bae et al's method, and also modify the first partial products to be determined based on the on the input data, the first output data, and the feedback data as an alternative mathematical manipulation as desired by the designer,

and to implement a reverse processing of the IDCT circuit as above so as to achieve a DCT/IDCT circuit for enabling forward and inverse discrete cosine transform of a data block as an incentive to utilize the IDCT circuit for multiple purposes, thereby saving extra costs associated with implementing a DCT circuit.

Regarding claims 18, 28, and 31, Bae et al discloses a sequence generator (210, 510) coupled to each core.

Regarding claims 19, 29, and 32, the Examiner considers selecting four cores as a design choice. Therefore, it would have been obvious to select four cores as long as the ends results are desirable by the product designer.

Regarding claim 20, the Examiner takes official notice that it is conventionally well known such as in the MPEG video compression/encoding scheme comprising of MEC engine comprising a data block including prediction data communicatively coupled to the DCT circuit so that the DCT circuit can perform DCT operation based on the prediction data received from the MEC engine.

Therefore, it would have been obvious to utilize conventional MEC engine being coupled to the DCT circuit so as to perform variety of tasks such as motion compensation/estimation as needed/desired by the conventional compressor/encoder.

Regarding claim 21, the Examiner takes official notice that it is conventionally well known such as in the MPEG video decompression/decoding scheme comprising of inverse quantizer module comprising a data block including reconstructed data communicatively coupled to the IDCT circuit so that the IDCT circuit can perform inverse DCT operation based on the reconstructed data received from the inverse quantizer module.

Therefore, it would have been obvious to utilize conventional inverse quantizer module being coupled to the IDCT circuit so as to perform inverse quantization as needed/desired by the conventional decompressor/decoder.

Regarding claim 22, the Examiner considers utilizing eight cores as a design choice. Therefore, it would have been obvious to utilize eight cores as long as the ends results are desirable by the product designer.

Regarding claim 23, the Examiner takes official notice that a plurality of cores comprising different (4) types of cores is conventionally well known in the art.

Therefore, it would have been obvious to utilize different types of core for the each core so as to perform a variety of task, respectively, as needed/desired.

Regarding claim 24, Bae et al discloses a type of core including a main register (230) for storing the feedback data.

Even though Bae et al's core does not include a main register for storing input data, Bae et al discloses an input memory (710) for storing the input data, which is subsequently used by the IDCT core.

Therefore, it would have been obvious to re-locate the input memory to be included in the core for storing the input data as an added convenience.

Regarding claim 39, the Examiner considers obtaining the final result within two clock cycles as a design choice. Furthermore, manipulating the timing cycles of the computation process for an efficient operation is well known in the art.

Therefore, it would have been obvious to obtain the final result within two clock cycles as long as the ends results are desirable by the engineer.

4. Claims 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bae et al (6,421,695 B1) in view of Asano (5,361,220).

Regarding claims 25-26, Bae et al does not particularly disclose a type of core including a first pair, a second pair, and two pairs of lookup tables.

However, Asano teaches DCT with reduced components comprising a plurality of lookup tables (Columns 16-25; TABLES 1-16).

Therefore, it would have been obvious to a person of ordinary skill in the relevant art employing an IDCT circuit for enabling inverse discrete cosine transform of a data block as taught by Bae et al to incorporate Asano's teaching as above for reducing components, thereby saving extra costs associated with additional components.

Allowable Subject Matter

5. Claim 40 is allowed.

6. The following is an examiner's statement of reasons for allowance:

claim 40 recites the novel feature of a system, comprising:

a DCT/IDCT circuit for enabling forward and inverse discrete cosine transform of a data block, comprising:

means for receiving input data associated with the data block;

coupled to the means for receiving, first means for selecting one of the input data and a sum of the input data and feedback data to provide first output data;

coupled to the first means, second means for determining a sum of partial products based on the input data, the feedback data, and first coefficient data to provide second output data;

coupled to the means for receiving input data, third means for determining a sum of second partial products based on the input data, the feedback data, and second coefficient data to provide third output data;

coupled to the means for receiving input data, fourth means for determining a sum of additional partial products based on the input data, the feedback data, and additional coefficient data to provide third output data; and

means for outputting the first output data, the second output data and the third output data collectively representing a result of one of the forward discrete cosine transform and inverse discrete cosine transform.

The art of records fail to anticipate or make obvious the novel features discussed as above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

A) Imanishi et al (6,243,735 B1), Microcontroller, data processing system and task switching control method.

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Shawn S An whose telephone number is 703-305-0099. The Examiner can normally be reached on Flex hours (10).

9. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SSA
Primary Patent Examiner
10/29/04